Remarks

Applicant appreciates the Examiner's indicating allowable subject matter in claims 5, 9 and 11.

Applicant cancelled claim 5 and added its subject matter to claim 1. Applicant deleted the word "layer," and the subject matter "by blanket epitaxy" from claim 1.

Applicant added new dependent claim 23, which re-presents the subject matter deleted from claim 1.

Accordingly, Applicant believes that any rejection under 35USC112 is overcome, and that claims 1-4, 6-11 and claim 23 are allowable.

Neither Taka et al., nor Chen et al., applied either singly or in combination, teaches, discloses or suggests "the semiconductor intrinsic base layer includes silicon germanium."

Entry and allowance of claims 1-4, 6-11, 23 are solicited.

Respectfully submitted,

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WHAT IS CLAIMED IS:

1. (Currently Amended) A bipolar transistor, comprising:

a substrate;

a semiconductor intrinsic base layer formed ~~by blanket epitaxy~~ on the substrate;

a collector layer formed on the substrate, wherein the semiconductor intrinsic base layer includes silicon germanium;

an emitter formed over the semiconductor intrinsic base layer, forming a junction between the semiconductor intrinsic base layer and the emitter, wherein the junction at a lateral portion of the emitter extends farther into the intrinsic base layer than the junction at a center portion of the emitter;

an extrinsic base formed adjacent to the lateral portion of the emitter;

a base electrode formed on a portion of the extrinsic base layer;

a collector electrode formed on a portion of the collector layer; and

an emitter electrode formed on a portion of the emitter ~~layer~~.

2. (Currently Amended) ~~A~~ The bipolar transistor as claimed in claim 1, wherein the emitter comprises a pedestal having a top which contacts an emitter layer.

3. (Currently Amended) ~~A~~ The bipolar transistor as claimed in claim 1, wherein a raised extrinsic base layer is formed and comprises one of a highly-doped polysilicon or a highly-doped amorphous silicon.

4. (Currently Amended) ~~A~~ The transistor ~~as recited~~ claimed in claim 1, wherein the lateral portion has a depth in a range of approximately 20-40 nm.

5. (Cancelled)

6. (Currently Amended) ~~A~~ The bipolar transistor as ~~recited~~ claimed in claim 1, further comprising a sidewall spacer formed between and electrically isolating the emitter and the extrinsic base layer.

7. (Currently Amended) ~~A~~ The bipolar transistor as ~~recited~~ claimed in claim 6, wherein the sidewall spacer comprises one of a silicon nitride, a silicon dioxide, or a combination of the two.

8. (Currently Amended) ~~A~~ The bipolar transistor as ~~recited~~ claimed in claim 7, wherein the sidewall spacer has a width in the range of 10 to 70 nanometers.

9. (Currently Amended) ~~A~~ The bipolar transistor as ~~recited~~ claimed in claim 2, wherein the emitter comprises one of a polysilicon or an amorphous silicon.

10. (Currently Amended) ~~A~~ The bipolar transistor as ~~recited~~ claimed in claim 1, wherein the emitter layer has a thickness in the range of 30 to 200 nanometers.

11. (Currently Amended) ~~A~~ The bipolar transistor as ~~recited~~ claimed in claim 1, wherein the emitter is in-situ doped with phosphorous that minimizes drive-in and activation anneal temperatures.

Claims 12 -22 (Withdrawn)

23. (New) The transistor as claimed in claim 1, wherein the semiconductor intrinsic base layer is formed by blanket epitaxy.